## WHAT IS CLAIME. S:

| 1          | 1. A method of fabricating a semiconductor device in a silicon on                                  |  |  |
|------------|--|--|--|
| 2          | insulator (SOI) substrate comprising the steps of:   |  |  |
| 3          | <ul> <li>a) providing a semiconductor body including a silicon supporting</li> </ul>               |  |  |
| 4          | substrate, a silicon oxide layer supported by the substrate, and a silicon layer overlying the     |  |  |
| 5          | silicon oxide layer;   |  |  |
| 6          | b) forming a semiconductor component in the silicon layer over a portion                           |  |  |
| 7          | of the silicon oxide layer;  |  |  |
| 8          | c) forming an etch mask on a surface of the substrate opposite from the                            |  |  |
| 9          | component;   |  |  |
| 10         | d) applying a preferential etchant to selectively etch the silicon in the                          |  |  |
| 11         | substrate underlying the portion of the silicon oxide layer; and                                   |  |  |
| 12         | e) providing a metal layer in the etched portion of the substrate to provide                       |  |  |
|            | heat removal from the component during operation of the component.                                 |  |  |
| <u></u>    | 2. The method as defined by claim 1 wherein the metal layer comprises a                            |  |  |
| <u>F</u> 2 | refractory metal.  |  |  |
| _          | The method as defined by claim 2 wherein the metal layer further                                   |  |  |
| # 2        | comprises gold, copper or aluminum over the refractory metal.                                      |  |  |
|            | The state of the refractory metal  |  |  |
| 1          | 4. The method as defined by claim 3 wherein the refractory metal                                   |  |  |
| <b>2</b>   | comprises titanium tungsten or titanium nitride.   |  |  |
| 1          | 5. The method as defined by claim 1 wherein step c) includes forming a                             |  |  |
| 2          | silicon nitride layer on the surface of the substrate and then preferentially masking and          |  |  |
| 3          | etching the silicon nitride layer to expose the silicon in the substrate underlying the portion of |  |  |
| 4          | the silicon oxide layer.   |  |  |
| 1          | 6. The method as defined by claim 5 wherein the silicon nitride layer is                           |  |  |
| 2          | preferentially etched with a dry plasma, and the silicon is preferentially etched with             |  |  |
| 3          | potassium hydroxide.   |  |  |
| 3          | 17   |  |  |
| 1          | 7. The method as defined by claim 6 wherein the silicon nitride is                                 |  |  |
| 2          | preferentially etched with a plasma and the silicon is preferentially etched with a plasma.        |  |  |
|            | <b>I</b>   |  |  |

| 1           | 8.                           | The method as defined by claim 5 and further including a step after           |  |
|-------------|------------------------------|---|--|
| 2           | step d) of preferentia       | ally etching the exposed portion of the silicon oxide layer.                  |  |
| 1           | 9.                           | The method as defined by claim 8 wherein the silicon oxide layer is           |  |
| 2           | etched with a buffer         |   |  |
| 2           | etched with a buller         | cum acid.   |  |
| 1           | 10.                          | The method as defined by claim 8 wherein the silicon oxide layer is           |  |
| 2           | etched with an ion p         | olasma.   |  |
|             | 11                           | The method as defined by claim 1 and further including a step after           |  |
| 1           | 11.                          | 1   |  |
| 2           | step d) of preferenti        | ally etching the exposed portion of the silicon oxide layer.                  |  |
| 1           | 12.                          | The method as defined by claim 1 and further including a step before          |  |
| 2           | step c) of abrading          | the substrate surface opposite from the component to reduce the thickness     |  |
| 3           | of the supporting substrate. |   |  |
|             |                              |   |  |
| ]<br>Fi     | 13.                          | The method as defined by claim 1 wherein step a) includes providing a         |  |
| 2           | bonded silicon on in         | nsulator wafer.   |  |
|             | 14.                          | The method as defined by claim 1 wherein step a) comprises providing          |  |
| 2           | a silicon wafer with         | implanted silicon oxide layer therein.  |  |
| -il≥        | 2                            |   |  |
| 1           | SUB 15.                      | A semiconductor device comprising:  |  |
| 1<br>2<br>3 | A1 / a)                      | a semiconductor body including a silicon supporting substrate, a              |  |
| 3           | silicon layer suppor         | rted by the substrate, and a silicon layer overlying the silicon oxide layer, |  |
| 4           | b)                           | a semiconductor component formed in the silicon layer overlying a             |  |
| 5           | portion of the subst         | trate which has been removed by etching, and                                  |  |
| 6           | c)                           | a metal layer in the portion of the substrate removed by etching, the         |  |
| 7           | metal layer providi          | ng heat removal from the component.   |  |
|             | 16                           | The semiconductor device as defined by claim 15, wherein the silicon          |  |
| 1           | 16.                          |   |  |
| 2           |                              | ng the portion of the substrate is removed, the metal layer abutting the      |  |
| 3           | silicon layer.               |   |  |
| 1           | 17.                          | The semiconductor device as defined by claim 16, wherein the metal            |  |
| 2           | layer comprises a r          | refractory metal.   |  |

| 1    | 18.                     | The semiconductor device as defined by claim 17, wherein the metal |
|------|-------------------------|--|
| 2    | layer comprises gold,   | aluminum or copper over the refractory metal.                      |
| 1    | 19.                     | The semiconductor device as defined by claim 17, wherein the       |
| 2    | refractory metal is tit | anium tungsten or titanium nitride.                                |
| 1    | 20.                     | The semiconductor device as defined by claim 15, wherein the metal |
| 2    | layer abuts the silicor | oxide layer.   |
| 15   | 21.                     | The semiconductor device as defined by claim 20, wherein the metal |
| 2    | layer comprises a refi  | ractory metal.   |
| 1    | 22.                     | The semiconductor device as defined by claim 21, wherein the metal |
| 2    | layer comprises gold    | over the refractory metal.   |
| 1    | 23.                     | The semiconductor device as defined by claim 21, wherein the       |
|      | refractory metal comp   | prises titanium tungsten.  |
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